

# **QUALIFICATION PLAN**

### PCN #: JAON-010MGE290

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# Qualification of GTK assembly site as an additional site for selected products in 8L SOIC package.

Distribution

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Purpose:	Qualification of GTK assembly site as an additional si					
-	for selected products in 8L SOIC package.					

- MP code:\_\_\_\_\_ DEDX2
- Part No.: \_\_\_\_\_ 24LC512
- BD No:\_\_\_\_\_ BDM-000730 rev.A
- CCB No.: 1565.01

#### Package:

Туре	_8L SOIC
Width or Size	_150 mils
Die thickness:	_15 mils
Die size:	_78.7 x 111.0 mils

### Lead frame:

_95 x 130 mils
_CDA194
_Ag spot
_Stamp
_No
_11-0208N-030
None
_Au
_CRM-1076DJ-G
_Yes
_G600
_Matte tin

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Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Standard Pb-free: Matte tin/ NiPdAu finish, SAC solder, wetting temp 245°C for both SMD & through hole packages.	22	5	1	27	> 95% lead coverage	5	Standard Pb-free solderability is the requirement. SnPb solderability (backward solderability—SMD reflow soldering) is required for any plating related changes and highly recommended for other package BOM changes.
Standard SnPb Solderability	JESD22B-102E; Perform 8 hour steam aging prior to testing. Standard SnPb: SnPb finish, SnPb solder, wetting temp 215°C for SMD & 245°C for through hole packages.	22	5	1	27	> 95% lead coverage	5	
Backward Solderability	JESD22B-102E; Perform 8 hours steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Backward: Matte tin/ NiPdAu finish, SnPb solder, wetting temp 215°C for SMD.	22	5	1	27	> 95% lead coverage	5	
Wire Bond Pull - WBP	Mil. Std. 883-2011	5	0	1	5	0 fails after TC	5	30 bonds from a minimum of 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001	5	0	1	5	0	5	30 bonds from a minimum of 5 devices.
Physical Dimensions	Measure per JESD22 B100 and B108	10	0	3	30	0	5	
External Visual	Mil. Std. 883-2009/2010	All devices prior to submission for qualification testing	0	3	ALL	0	5	
HTSL (High Temp Storage Life)	+175 C for 504 hours or 150°C for 1008 hrs. Electrical test pre and post stress at +25C and hot temp.	45	5	1	50	0	10	Must be in progress at time of package release to production, but completion is not required for release to production.
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Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Preconditioning - Required for surface mount devices	+150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020D for package type; Electrical test pre and post stress at +25°C. MSL-1 @ 260°C	231	15	4	984	0	15	Spares should be properly identified. 77 parts from each lot to be used for HAST, Autoclave, Temp Cycle test.
HAST	+130°C/85% RH for 96 hours. Electrical test pre and post stress at +25°C and hot temp. 1 lot tested at 125C	77	5	4	328	0	10	Spares should be properly identified. Use the parts which have gone through Pre- conditioning.
Unbiased HAST	+130°C/85% RH for 96 hrs	77	5	4	328	0	10	Spares should be properly identified. Use the parts which have gone through Pre- conditioning.
Temp Cycle	-65°C to +150°C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress. 1 lot tested at 125C	77	5	4	328	0	15	Spares should be properly identified. Use the parts which have gone through Pre- conditioning.